The Bally FPGA code is now complete, and available for download here. (Scroll all the way down). Hi-Res is now supported along with additional memory - 28K RAM in this case. External cartridges are also supported using the Intel StrataFlash on the board. Below is an example of the Treasure Cove game running.



This version will run on a Xilinx Spartan3E starter kit board. The distribution includes a pre-built build\bally.bit file which can be downloaded to the board

See the <u>Space Invaders page</u> page for details on the audio output required, and the <u>Platforms/Display test page</u> for details on how to modify the board to increase the colour resolution.

Details of how the switches etc on the Spartan3e starter board are in the README.TXT.

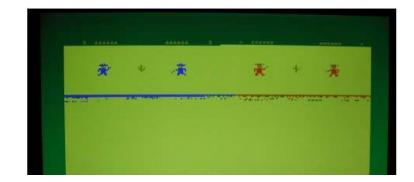
Switch0 (bottom right) is used to switch between NTSC (15KHz) output and VGA(31KHz).

Switch1 when up (on) will DISABLE the external flash memory (unplug cart).

Switch3 and 2 are a two bit bank select to the flash memory.

The push button on the rotary control is used for reset.

I don't have any hi-res software, but here is Gunfight running in forced hi-res mode. The VHDL code is based on measurements of real chips, so I wanted to implement hi-res with as few changes as possible. I expanded the RAM data width to 16 bits. CPU RAM access and low-res mode screen reads are still 8 bit to either the lower or higher 8 bits. For hi-res I shift the address up one bit (so the lower bit is always 0) and use all 16 bits.



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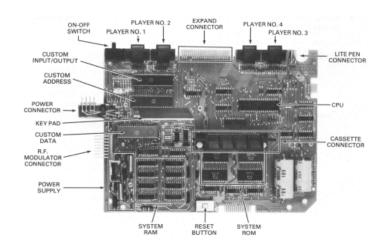
To program the flash you can use the very nice PicoBlaze RS-232 StrataFlash programmer by the great Ken Chapman :

www.xilinx.com/products/boards/s3estarter/reference_designs

The PicoBlaze design from Xilinx uses the female RS-232 connector on the Starter kit board. I have modified it to use the male connector, then you can use a standard female-to-female null modem cable with a pin 2-3 swap. s3esk_picoblaze_nor_flash_programmer_female.bit

The original hardware:

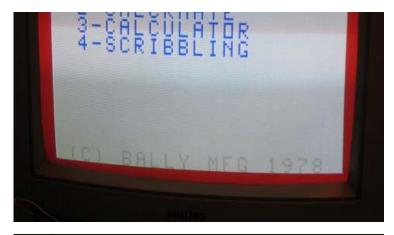
SYSTEM BLOCK DIAGRAM Z-80 CPU ADDRESS 4 K BYTE RAM UB-UIC U24-U3I 8K BYTE SYSTEM RF DATA CH. 3 OR 4 TO T. V. RECEIVER CHIP ROM UI-U4 8K BYTE CONTROL I/O CHIP 24 BUTTON CASSETTE KEYPAD ROM (1-4)IEEE EXPANDER BUS



Pictures taken from the code here running:



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Please read the "README" file for documentation.

IMPORTANT NOTE:

BIOS ROM CONTENTS ARE INCLUDED IN THIS DISTRIBUTION.

A simulation model of Bally Astrocade hardware Copyright (c) MikeJ - October 2006

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You are responsible for any legal issues arising from your use of this code.

You must agree to this disclaimer before downloading the code

Version 004 Hi_Res bally_rel004_sp3e_hires.zip

17 1 000 /m 1 1 1 1 1 1000 0 1

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Version 003 (Previous_version) bally_rel003_sp3e.zip

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